This quality specification applies to all Celestica PCB prototype and production orders. The supplier is required to comply with all sections of this document. Please contact Celestica before proceeding with the order if a discrepancy is found between this Q-spec and the applicable drawings and specifications.

A. PART INFORMATION:

Celestica Part Number: _____As Above_____

Supplier Part Number: _____As Above_____

Date: _____As Above_____

B. CARD FINISH:

The surface finish shall be as noted in the board fabrication data (ie. fab drawing, gerber data, readme file, etc.) unless specified below in the Special Instructions. If any discrepancy is noted, please contact a member of the engineering team provided above or the Celestica buyer for resolution.

C. SPECIAL INSTRUCTIONS:

1) When delivering to ASIA sites: Supplier shall provide one set of supplier modified a/w film and one set of master a/w film in the first shipment.

2) For every shipment the supplier shall complete Section G (First Article/Ship Lot Audit Report) of this document and provide it along with the Certificate of Compliance. These documents are to be included in a clearly marked box on the top of the pallet.

3) If parts are ROHS compliant, it should be clearly stated on the CofC.

4) 2 soldersamples shall be included with each shipment. These samples may be non-functional (rejected for minor cosmetic defects or opens /shorts) provided that they are representative of the lot and a detailed description is provided stating the reason for its rejection. These samples may be used for incoming testing to confirm the quality of the product and to accept/reject the shipment.

5) Contact our engineering if S/M Taiyo PSR4000-Z100 is used since it may be incompatible with fluxes used within Celestica mfg.

6) DO NOT SHIP X-OUTS (Partially Good Panels) without prior written approval from Celestica Purchasing Authority.

D. PANEL DRAWING (where applicable)

Panelization drawing #:
Other:

Note: If panelization drawing is not specified, please contact Celestica buyer to determine whether required.

E. APPLICABLE SPECIFICATIONS:
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1) As referenced on the part specific drawings

2) Celestica PWB Specification: CELQ-001-SPEC-2 (latest revision)

F. SUPPLIER FIRST ARTICLE/SHIP LOT AUDIT REPORT:

The supplier shall complete the following report after the final inspection. THE SUPPLIER MAY USE THEIR OWN FORMAT for this report provided that it includes ALL data requested in this section, if this report is used, pictures of the microsection must be attached.

Date: _____

Supplier P/N: _____ Rev_____

Supplier Name & Location: _____

Celestica P/N: _____

Purchase Order: _____

Date Code(s): _____

Lot Number(s): _____

Base material type & manufacturer: _____

Report Prepared by (Name & signature): _____

_____

1) VISUAL INSPECTION

Sample size: A minimum of 50 cards (or panels if cards are panelized) or 1% of the shipment (whichever is greater) from randomly selected panels in the shipment.

For orders less than 50 pcs, the sample size defaults to the full quantity

Verify P/N and revision on actual card
Result (Pass/Fail): _____

General inspection to be performed with 3 diopters dazor must check for:
- Burrs
- Nicks
- Haloing
- Weave Texture/Exposure, Measling, Crazing
- Pits, Dents, Voids
- Delamination/Blister
- Inclusions
- Lifted Lands
- Marking (Etched/Screened/Stamped)
- Soldermask coverage
- Soldermask registration
- Soldermask blisters/delamination
- Soldermask adhesion (tape test required)
- Soldermask plug, Via tenting

Observations/Comments: _____
_____
Result (Pass/Fail):_____

Contact tab inspection to be performed with 10X stereoscope
Result (Pass/Fail):_____

Warpage (%)
Method used: _____
Requirement: _____
Actual result: _____
Result (Pass/Fail): _____

Note: No physical manipulation of the board is allowed in order to meet flatness requirements. No thermal manipulation of boards is allowed without first obtaining written approval from Celestica.

2) DIMENSIONS

Sample Size: 3 randomly selected panels

Celestica considers all dimensions on the print to be critical to the function of the card. Dimensions are to be checked to the original prints, not to supplier generated artwork or milling programs.

The following must be checked:
- Outline drawing dimensions
- Panel drawing dimensions

Please include the fabrication drawing used referencing the locations of all dimensions measured and included in the table below.

Specify Method Used: Vernier or CMM
Units of Measure(must be the same as dwg):

Dimension #	Nominal	Tolerance	Actual	Pass/Fail

Card Thickness (4 locations)
Method used: Vernier or CMM
Units of Measure(must be the same as dwg):
Measurement taken over metal or soldermask:

Nominal	Tolerance	Actual	Pass/Fail

Hole Size Audit

Each hole size stated on the fabrication drawing shall be measured at least once. Holes should be measured in a high current density area. Special tolerances may be stated for press fit holes.

Units of Measure(must be the same as dwg):

Hole Diameter	Tolerance	Actual	Pass/Fail

3) PLATING THICKNESS (XRF)

Two measurements (one top, one bottom) on each of 10 randomly selected panels.

Note: Before XRF readings are performed supplier shall measure a calibration reference sample.

Finish/Metalisation Type:
Units of Measure:

Sample #	Max Thickness	Min Thickness	Actual	Pass/Fail
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____

Tape test on all plating types & soldermask
Note: Please perform tape test in a high-density area
Method used: _____
Result (Pass/Fail) for plating: _____
Result (Pass/Fail) for soldermask: _____

4) X-SECTION: 2 randomly selected panels

All dielectric and copper weights to be verified.

Soldermask thickness (measured over copper) to be verified.
Result (provide value): _____

Layer#	Dielectric Thickness Required	Dielectric Thickness Actual	Plies used	Pass/Fail	Layer#	Copper Thickness Required	Copper Thickness Actual	Pass/Fail
1-2					1			
2-3					2			
3-4					3			
4-5					4			
5-6					5			
6-7					6			
7-8					7			
8-9					8			
9-10					9			
10-11					10			
11-12					11			
12-13					12			
13-14					13			
14-15					14			
15-16					15			
16-17					16			
17-18					17			
18-19					18			
19-20					19			
20-21					20			
21-22					21			
22-23					22			
23-24					23			
24-25					24			
25-26					25			
26-27					26			
27-28					27			
28-29					28			
29-30					29			
					30			

PTH Copper Plating

Minimum Cu plating thickness required: _____
Minimum average Cu plating thickness required: _____

Cu thickness readings shall be:
- measured in a low current density area
- to be taken at 6 locations within the barrel:

Barrel Position

	Measurement #1	Measurement #2
Top	_____	_____
Middle	_____	_____
Bottom	_____	_____

Average: _____

Result (Pass/Fail): _____

Microsections are to be taken from a group of thermally stressed plated-through holes at the diameter of the holes, at 90 degrees to the board surface. Boards are to be thermally stressed with a 6X solder float test (500F solder pot with 10 sec float time for each float) X-section of 6x solder float test board (550 deg F solder pot with 10 seconds immersion time for each immersion).

- 3 samples must be taken diagonally across the board for the smallest via holes on the card including a high via density area (ie. BGA). A minimum of 6 holes per sample shall be evaluated.
- 1 sample must be taken of the largest plated through hole by volume (ie. connector area) per lot.
- Microsections should also include one hole of each type used in the design (eg. PTH, microvia, blind, buried, etc.)

A photograph of each hole type microsection (as stated above) must be included in the report.

General inspection for barrel integrity to verify the following conditions meets acceptability criteria:
- Laminate voids
- Registration
- Delamination/Blister
- Resin recession
- Foil/Plating cracks
- Conductor cracks
- Etchback/Smear removal
- Minimum annular ring
- IP Separation
- Wicking
- Lifted lands
- Plating nodules/burrs
- Plating folds

Observations/Comments: _____
_____
Results (Pass/Fail): _____

5) IONIC CLEANLINESS

Ionic contamination must be tested before soldermask and also after surface finish is applied.

Method used: _____
Results (provide value & units) after surface finish: _____

6) SOLDERABILITY TESTING

Please refer to J-STD-003. Testing is to be performed on both the surface and plated through holes. The pass criteria means that 95% of the individual pad surface area must wet.

Please include the coupon used for testing or a picture to illustrate the results.

Method used: _____
Results (Pass/Fail): _____

7) CONTROLLED IMPEDANCE

Data included with the report (Y/NA):_____

Note: If this board has controlled impedance (as specified on fab dwg), please retain supplier impedance results and coupons for a period of 24 months.[j1]

8) ELECTRICAL TEST

ET Fixture Type (Flying Probe or Bed of Nails): _____

Yields from the lot(s) included: _____

END OF FIRST ARTICLE